WHAT IS CLAIMED IS:

1. A DMX encoder, comprising:

a DMX input port configured to receive a DMX data stream having DMX data;

a level shifter configured to shift the DMX data stream to a TTL level;

a universal asynchronous receiver and transmitter configured to format the DMX data stream into a plurality of packets;

a digital signal processor configured to insert the plurality of packets into an AES digital audio stream to produce an encoded data stream carrying the DMX data;

an AES formatter configured to shift the encoded data stream to an unbalanced AES digital audio stream; and

a transformer configured to transform the unbalanced AES digital audio stream to a balanced AES digital audio stream.

2. The DMX encoder as defined in Claim 1, wherein the AES digital audio stream is received from the AES formatter.

3. The DMX encoder as defined in Claim 1, wherein the AES formatter is configured to generate the AES digital audio stream.

4. The DMX encoder as defined in Claim 1, further comprising an AES input port coupled to the AES formatter.

5. The DMX encoder as defined in Claim 4, wherein the AES formatter is configured to receive the AES digital audio stream from the AES input port.

6. The DMX encoder as defined in Claim 4, wherein the AES formatter is configured to receive an AES word clock signal that is derived from the AES input port.

7. The DMX encoder as defined in Claim 6, wherein the AES word clock signal synchronizes an output of the AES formatter.

8. A method of encoding a DMX data stream into a balanced AES digital audio stream, the method comprising:

receiving a DMX data stream having DMX data;

shifting the DMX data stream to a TTL level;

formatting the DMX data stream into a plurality of packets;

inserting the plurality of packets into an AES digital audio stream to produce an encoded data stream carrying the DMX data;

shifting the encoded data stream to an unbalanced AES digital audio stream; and

transforming the unbalanced AES digital audio stream to a balanced AES digital audio stream.

9. The method of encoding as defined in Claim 8, further comprising generating the AES digital audio stream.

10. The method of encoding as defined in Claim 8, further comprising receiving the AES digital audio stream.

11. The method of encoding as defined in Claim 8, further comprising receiving an AES word clock signal for synchronization.

12. A DMX decoder, comprising:

an AES formatter configured to receive an AES digital audio stream having a cyclic redundancy code value and DMX data;

a digital signal processor configured to receive the AES digital audio stream, to determine whether the cyclic redundancy code value is valid, and to extract the DMX data from the AES digital audio stream if the cyclic redundancy code value is valid and to retrieve stored DMX data if the cyclic redundancy code value is not valid;

a universal asynchronous receiver and transmitter configured to receive the DMX data; and

a level shifter configured to shift the DMX data to a DMX output level.

13. The DMX decoder as defined in Claim 12, wherein the AES formatter is further configured to convert the AES digital audio stream to a TTL level.

14. The DMX decoder as defined in Claim 12, wherein the AES formatter is further configured to verify that the AES digital audio stream is a valid AES stream.

15. The DMX decoder as defined in Claim 12, wherein the digital signal processor is further configured to store a plurality of DMX codes representing a particular scene.

16. The DMX decoder as defined in Claim 12, wherein the universal asynchronous receiver and transmitter is further configured to format the DMX data.

17. A method of decoding an AES digital audio stream into a DMX data stream, the method comprising:

receiving an AES digital audio stream having a cyclic redundancy code value and DMX data;

sending the AES digital audio stream to a digital signal processor;

determining whether the cyclic redundancy code value is valid;

if the cyclic redundancy code value is valid, then extract the DMX data from the AES digital audio stream, and

if the cyclic redundancy code value is not valid, then retrieve stored DMX data from the digital signal processor;

sending the DMX data to a universal asynchronous receiver and transmitter;

formatting the DMX data; and

shifting the DMX data to a DMX output level.

18. The method of decoding as defined in Claim 17, further comprising storing a plurality of DMX codes in the digital signal processor, the plurality of DMX codes representing a particular scene.

19. The method of decoding as defined in Claim 17, further comprising storing a plurality of scaler DMX codes in the digital signal processor.

20. The method of decoding as defined in Claim 19, wherein the digital signal processor compares the plurality of scaler DMX codes with the DMX output level to ensure that the DMX output level is not greater than one or more of the plurality of scaler DMX codes.

21. A distribution system, comprising:

a server configured to receive an encrypted digital data stream;

a decryption module configured to decrypt the encrypted digital data stream to produce a digital data stream;

a decoder configured to parse the digital data stream into a digital audio stream and a digital video stream and to send the digital video stream to a digital video projector;

a digital-to-analog converter configured to receive a first portion of the digital audio stream and to convert the first portion of the digital audio stream to analog audio; and

a decoder configured to receive a second portion of the digital audio stream, to extract a DMX code from the second portion of the digital audio stream, and to send the DMX code to equipment.